REMARKS

Claims 5-9 are now present in this application.

Claims 5-9 have been amended. Reconsideration of the application, as amended, is respectfully requested.

Claims 5-8 stand rejected under 35 USC 103 as being unpatentable over HARDEE, U.S. Patent 5,389,842, in view of IGARASHI, U.S. Patent 4,656,491, or STEUDEL, U.S. Patent 3,712,995. This rejection is respectfully traversed.

Claim 9 stands rejected under 35 USC 103 as being unpatentable over HARDEE, IGARARSHI, and STEUDEL, in view of KER et al., U.S. Patent 6,072,219. This rejection is respectfully traversed.

With regard to claim 5 of the present application, it is respectfully submitted that none of HARDEE, IGARASHI, or STEUDEL teaches, discloses or suggests that each of the MOS FETs has a source region of the first conductivity type directly connected to a power rail.

In the second paragraph of section 2, the Examiner asserts that:

> "Hardee teaches in figure 2 and related text an ESD protection component, comprising:…at least two MOS field effect transistors 26, 42…wherein each of the

MOS FETs has a source region of the first conductivity type coupled to a power rail,…"

However, in Fig. 2 of HARDEE, there is only one MOS FET 26 having a source region 24 directly connected to a power rail VCCEXT. The source region 44 of the other MOS FET 42 is not directly connected to a power rail.

Moreover, in the related text in col. 5, lines 33-35, HARDEE teaches that:

"Region 44 is coupled by a representative (conductive) line to provide the output signal of the integrated circuit device."

Accordingly, HARDEE does not teach that each of the MOS FETs has a source region of the first conductivity type directly connected to a power rail.

With regard to claim 7 of the present application, it is also respectfully submitted that none of HARDEE, IGARASHI, or STEUDEL teaches, discloses or suggests that the first doping region is directly connected to a pad.

In the second paragraph of section 2, the Examiner asserts that:

"Hardee teaches in figure 2 and related text an ESD protection component,

comprising:...a first doping area 34...wherein the first doping region...coupled to a pad,..."

However, in Fig. 2 of HARDEE, the doping area 34 is directly connected to the drain region 28 rather than a pad.

Moreover, in the related text in col. 5, lines 14-16, HARDEE teaches that:

"Region 34 is the source electrode of transistor 14 and is connected to N+ region 28 by a representative conductive line."

Accordingly, HARDEE does not teach a first doping region directly connected to a pad.

With regard to claim 8 of the present application, it is also respectfully submitted that none of HARDEE, IGARASHI or STEUDEL teaches, discloses or suggests that each of the MOS FETs has a drain region of the first conductivity type directly connected to a pad.

In the second paragraph of section 2, the Examiner asserts that:

"Hardee teaches in figure 2 and related text an ESD protection component, comprising:...at least two MOS field effect

> transistors 26, 42…wherein …each of the MOS FETs has a drain region of the first conductivity type coupled to a pad,…"

However, in Fig. 2 of HARDEE, neither drain region 28 nor 44 of the MOS FETs 26 and 42 is directly connected to a pad.

Moreover, in the related text in col. 5, lines 14-16 and lines 33-35, HARDEE teaches that:

> "Region 34 is the source electrode of transistor 14 and is connected to N+ region 28 by a representative conductive line"; and

> "Region 44 is coupled by a representative (conductive) line to provide the output signal of the integrated circuit device".

Accordingly, HARDEE does not teach that each of the MOS FETs has a drain region of the first conductivity type directly connected to a pad.

With regard to claim 6 of the present application, it respectfully submitted that none of HARDEE, IGARASHI, or STEUDEL teaches, discloses or suggests a first well electrically connected to a pad.

In the seventh paragraph of section 2, the office action states

> "Regarding to Claim 6, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect the pad to the first well through the extension areas in order to reduce the contact resistance of the device by connecting the enlarged contact area of the first well to the pad."

However, in Fig. 2 of HARDEE, the first well 22 is not directly connected to a pad.

Moreover, in the related text in col. 5, lines 21-25, HARDEE teaches

> "It will be seen that within region 22, an N+ diffusion or region 32 has been constructed. This region 32 is a heavily doped, preferably arsenic or phosphorus region that is electrically coupled to receive the voltage VCCP."

Accordingly, the well 22 taught by HARDEE is electrically connected to receive a voltage VCCP by a heavily doped region 32 but not electrically connected to a pad. HARDEE at most teaches a

region 32 coupling the well 22 to the voltage VCCP, rather than a pad, in order to reduce the contact resistance. It is unreasonable to allege that it is obvious to connect the pad to the first well only from HARDEE's teaching "the well 22 is electrically coupled to receive a voltage VCCP".

With regard to claim 9, it is respectfully submitted that none of HARDEE, IGARASHI, STEUDEL, or KER et al. teaches, discloses or suggests two MOS field effect transistors both having sources directly connected to a power supply, a doping area directly connected to a pad and a first well electrically connected to a pad.

In the second paragraph of section 3, the office action states

> "Hardee, Igarashi and Steudel teach substantially the entire claimed structure, as applied to claim 1 above..."

However, as previously described, HARDEE teaches the source region 44 of the MOS FET 42 being coupled to provide the output signal of the integrated circuit device rather than a power supply, and the first well 22 and doping area 34 respectively being coupled to receive a voltage VCCP and the N+ region 28 rather than a pad.

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims should now be in condition

for allowance. Reconsideration and withdrawal of the 35 USC 103 rejections are respectfully requested.

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

In the event the Examiner does not consider this application to be in condition for allowance, it is respectfully requested that this Amendment be entered for the purposes of Appeal. This Amendment should overcome the current grounds of rejection and therefore simplify the issues for Appeal. Nonetheless, it should be unnecessary to proceed to Appeal because the instant application should now be in condition for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Joe McKinney Muncy, #32,334

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

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Attachment(s)